

FLASH MEMORY DEVICE HAVING COLUMN PREDECODER CAPABLE OF  
SELECTING ALL COLUMN SELECTION TRANSISTORS AND STRESS TEST  
METHOD THEREOF

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ABSTRACT OF THE DISCLOSURE

Embodiments of the invention provide a flash memory device having a column  
predecoder for selecting all column selection transistors during a stress test, and also provide  
a stress test method for the flash memory device. An embodiment's column predecoder  
includes a buffer unit for inputting all column selection signals, decoder units for decoding an  
10 output of the buffer unit and column addresses, and level shifters for shifting voltage levels of  
column selection signals coupled to gates of the column selection transistors in response to an  
output of the decoder units. Since a ground voltage is applied to a bitline and a high voltage is  
applied to all column selection signals during the stress test, the stress test time can be  
shortened.